(a) SIGNAL IN → RF/IF AMPLIFIERS → DEMODULATOR → DECODING LOGIC → DATA OUT; SYNCHRONIZATION; f_1 CLK. #1; CLK #2 f_2; CLK #3 f_3

(b) RF/IF AMPLIFIERS → DEMODULATOR → DECODING LOGIC → DATA OUT; f_1 SYNCHRONIZATION; PLL; DIVIDER "A" f_2; DIVIDER "B" f_3

(c) SIGNAL IN → RF/IF AMPLIFIERS → DEMODULATOR → DECODING LOGIC → DATA OUT; SYNCHRONIZATION; PLL#1 f_1; PLL#2 f_2; PLL#3 f_3

f_1 = RF/IF carrier

f_2 = Bit rate

f_3 = Frame rate

Fig. 1 (Prior Art)

Fig. 2

Fig. 3

SIGNAL
IN — A

COMP.
IN — B

XOR
OUT — R — TO VCO INPUT
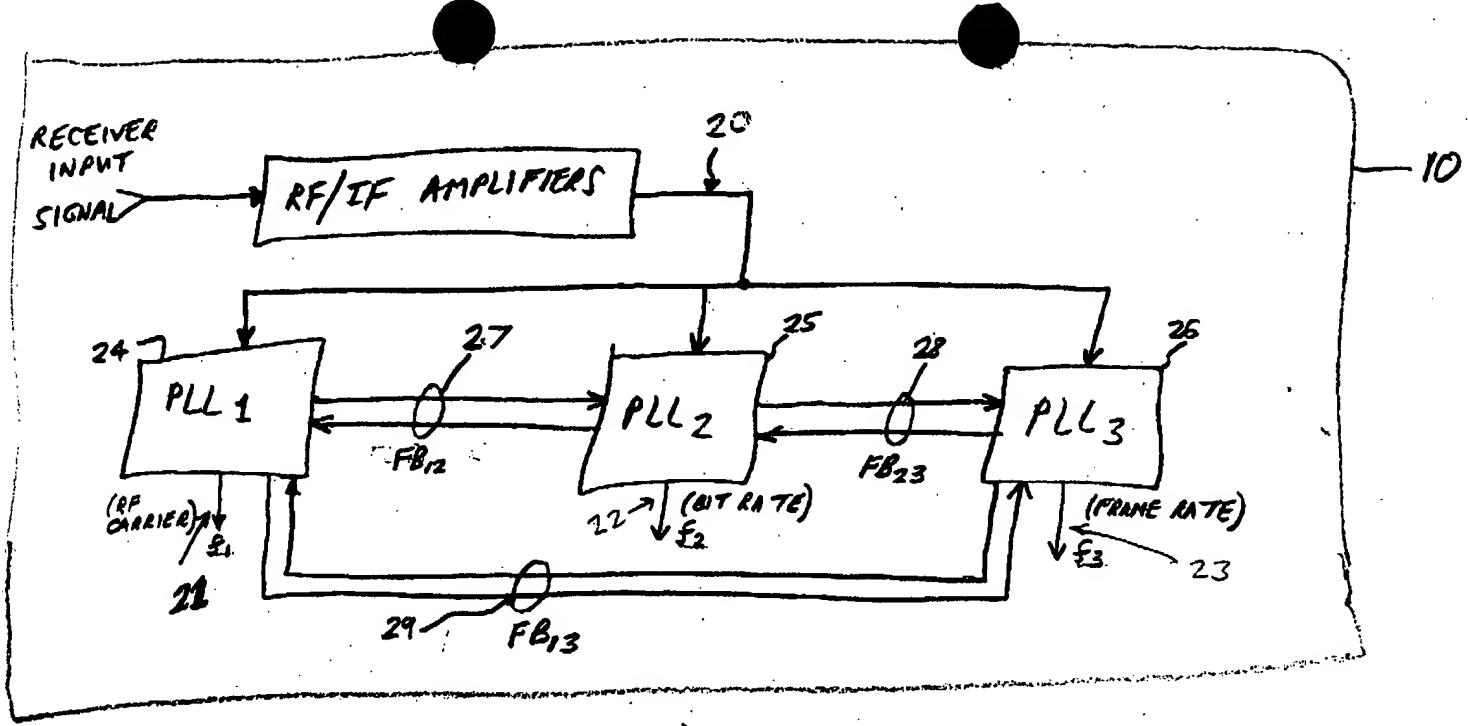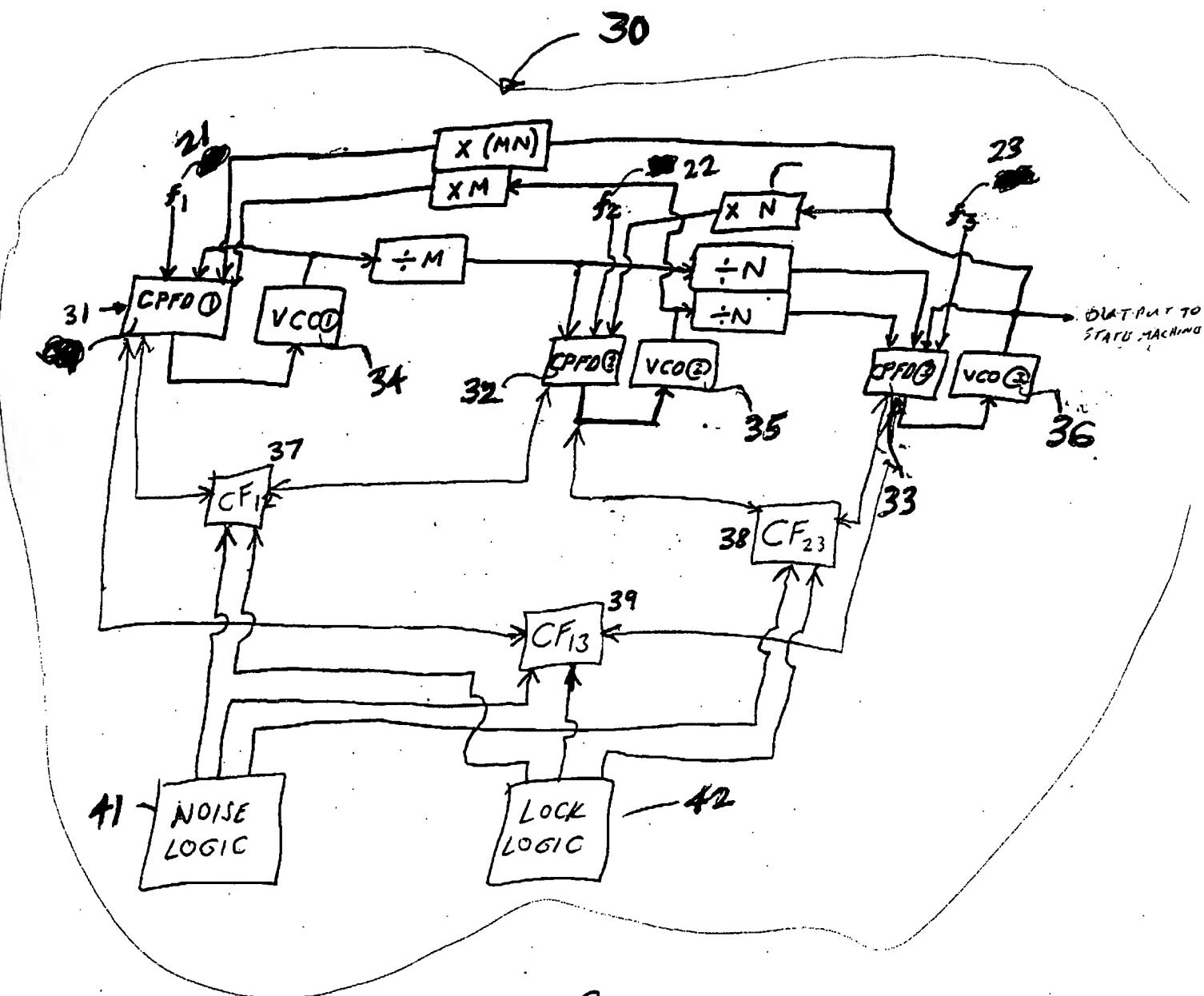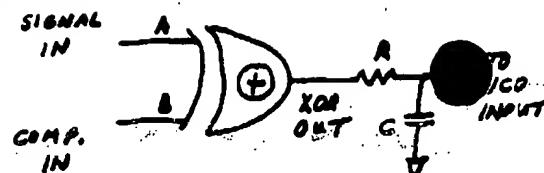
(A) Basic XOR Phase Comparator.

A	B	XOR
0	0	0
0	1	1
1	0	1
1	1	0

SIGNAL CO TIMING

SIGNAL (14) IN — TO OTHER COMPARATORS (4)

COMPARATOR (3) IN — TO OTHER COMPARATORS (5)

XOR PHASE OUTPUT (2)

INPUT CIRCUITRY COMMON TO ALL COMPARATORS
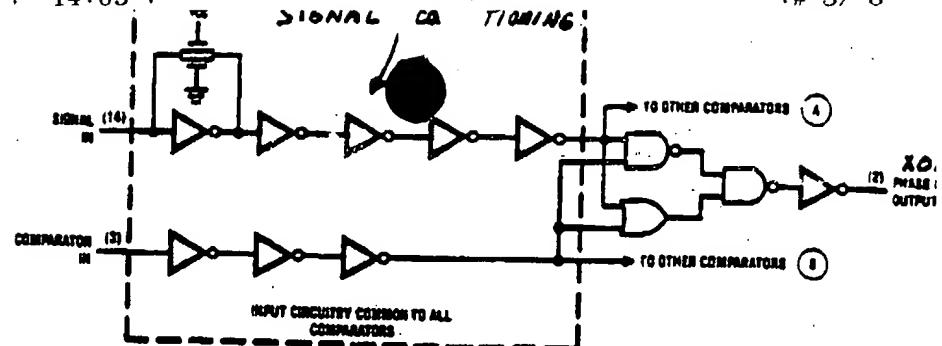
(B) Detailed on-chip IC circuitry in 74HC404

SIGNAL IN

COMPARATOR IN

PHASE COMPARATOR (XOR) OUTPUT

VCO IN
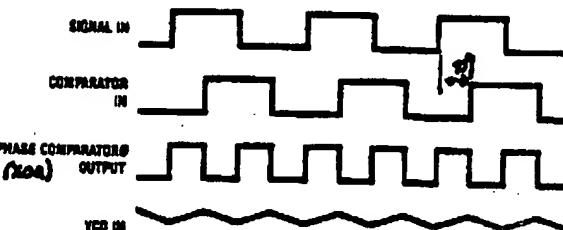
(C) Typical XOR Detector Waveforms.
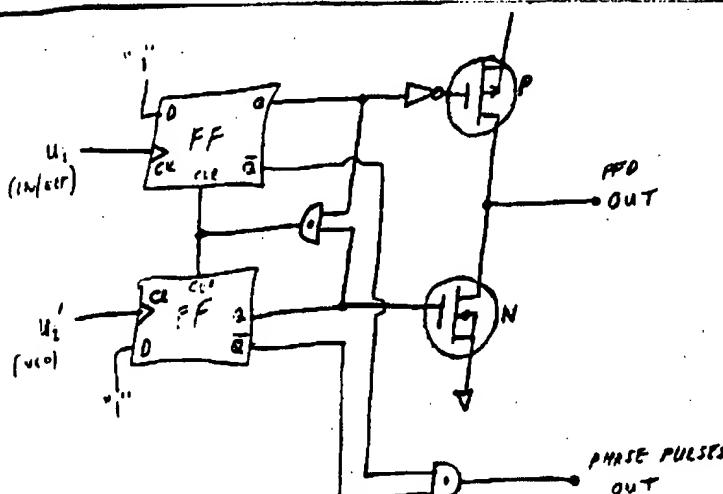
Uᵢ (IN/REF) — FF clr Q Q̄ — P

PFD OUT

Uᵢ' (VCO) — FF clr Q Q̄ — N

PHASE PULSES OUT

High-Level Diagram of PFD (existing art).

PHASE COMPARATOR INPUT CIRCUIT

(12) PHASE COMPARATOR B OUTPUT

(1) PHASE PULSES OUTPUT

PHASE COMPARATOR INPUT CIRCUIT

Gate-Level Diagram of PFD (existing art)

SIGNAL IN

COMPARATOR IN

COMPARATOR B OUT

VCO IN

PHASE PULSES
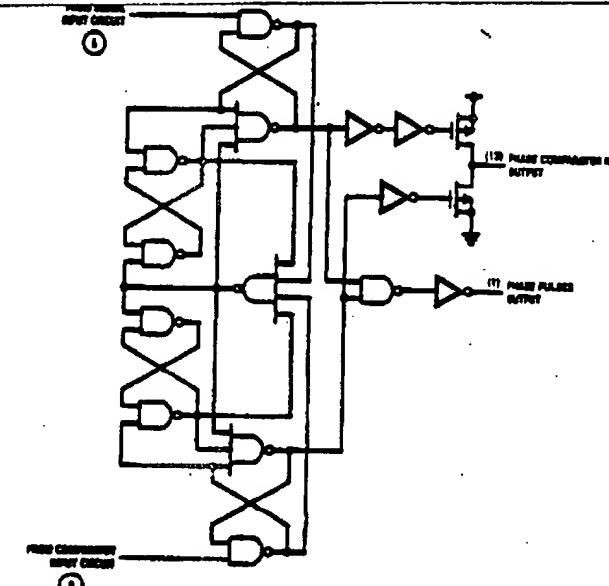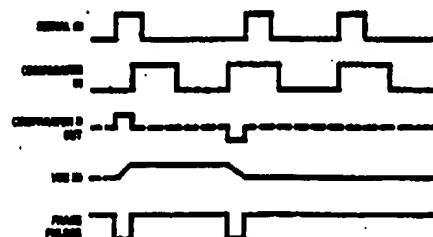
Timing and Waveforms of PFD (existing art).

Fig. 4 (Prior Art)

Fig. 5

Fig **6.** Typical Implementation of Input-Signal Noise Suppression.

GAIN ADJUST

Main Loop Amplifier

COMBINER CIRCUIT

VCO

f_{VCO}

$\frac{f_{VCO}}{f_1} = L$

LOOP COMPENSATION ADJUST

Loop Amplifier Gain = L

÷ L

31 CPFD₁

f_1

f_1 IN

$\frac{f_1}{f_2} = M$

Loop Amplifier Gain = L·M

÷ M

32 CPFD₂

f_2

f_2 IN

f_2

Loop Amplifier Gain = L·M·N

$\frac{f_2}{f_3} = N$

÷ N

33 CPFD₃

f_3

f_3 IN
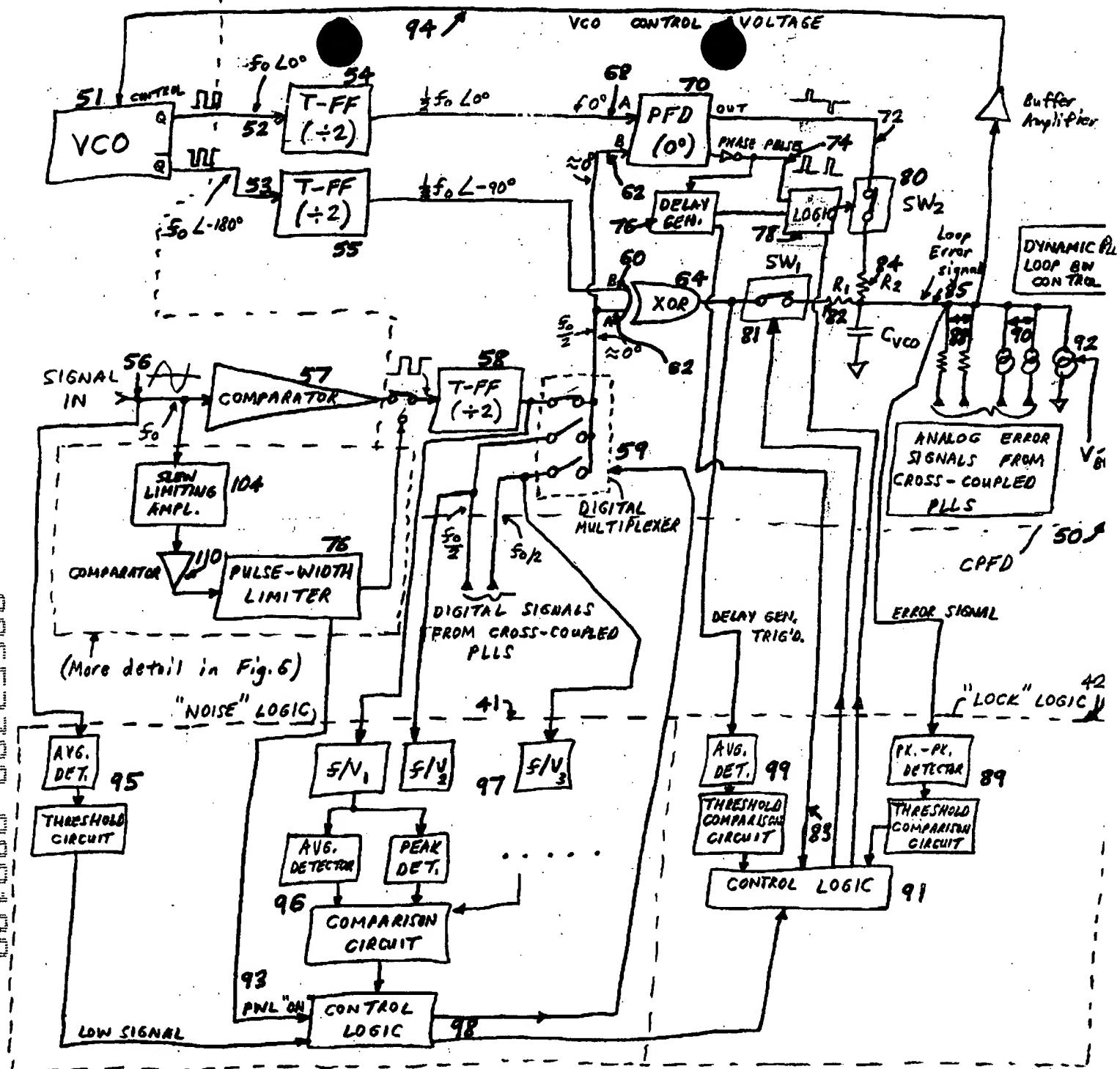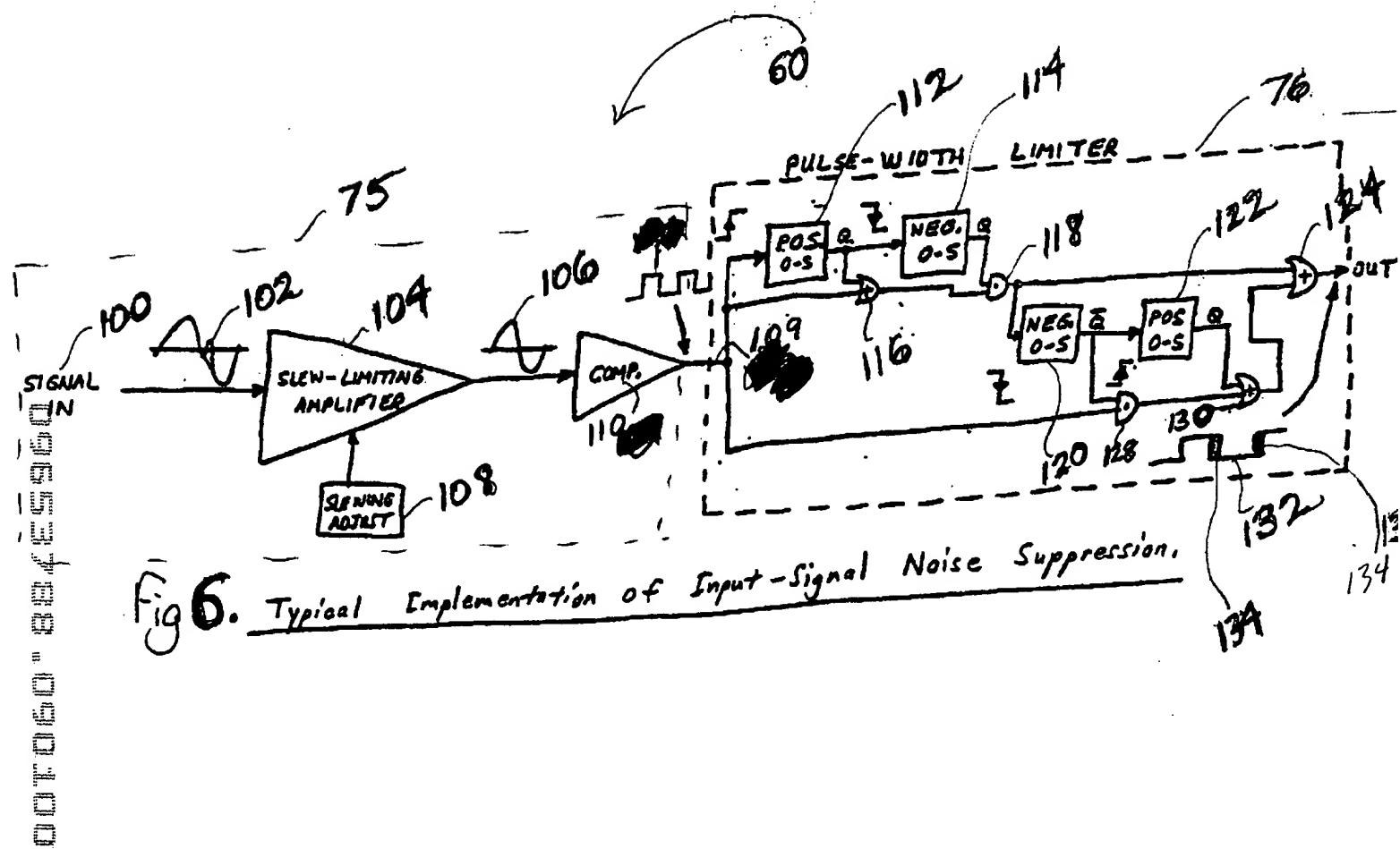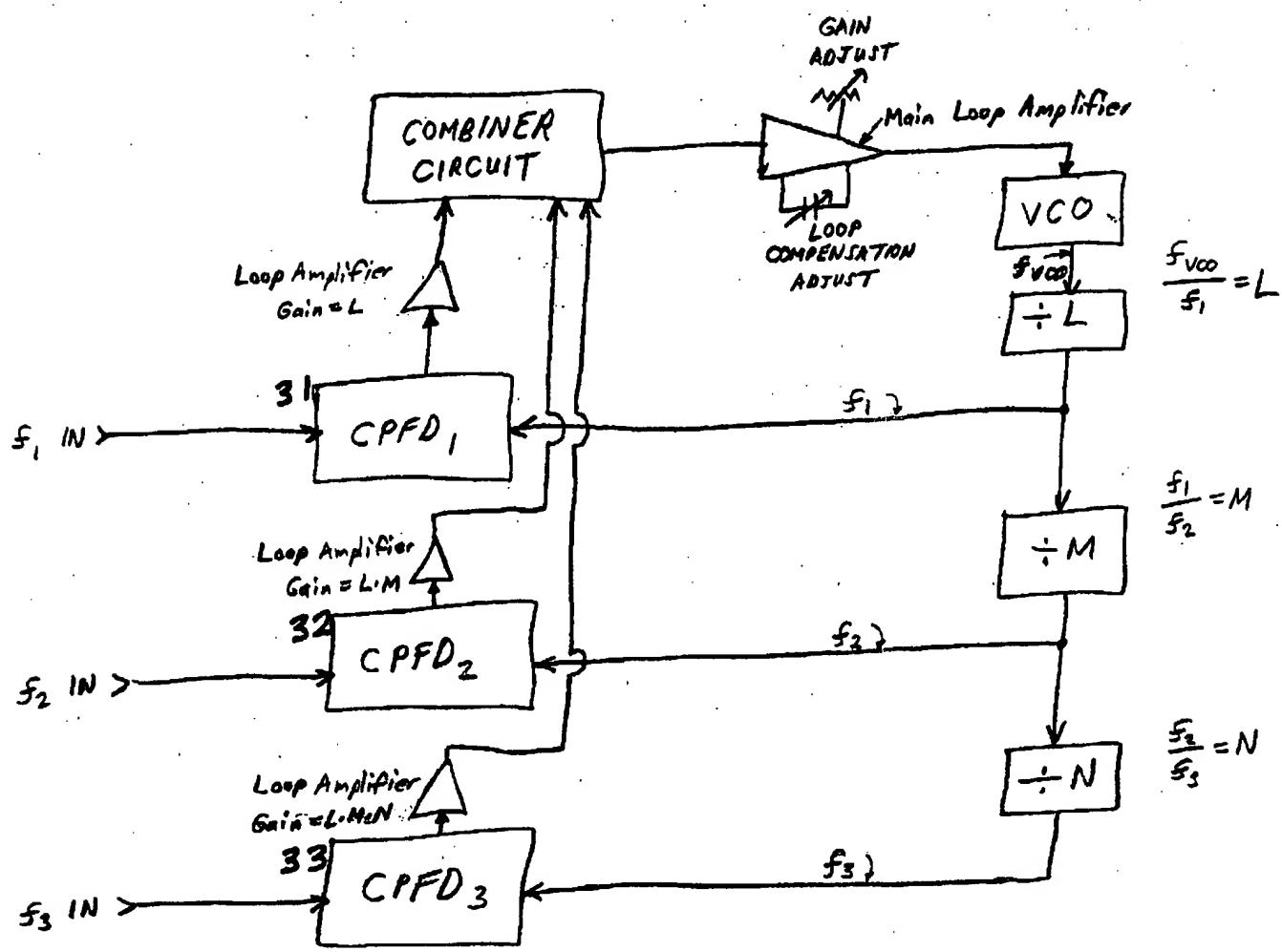
Fig. 7   Single-VCO System Implementation